Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1.   (Currently Amended) A̶n̶ single exclusive interface to transfer data directly between a memory control hub (MCH) and a input/output control hub (ICH) within a computer system, comprising:

a data signal path to transmit data in packets via split transactions; and

a set of command signals, wherein said interface provides a point-to-point connection between said MCH and said ICH, exclusive of an external bus connected directly to the interface, and peripheral components only connected to MCH via t̶h̶e̶ a single interface between the MCH and ICH.

2.   (Original) The interface of claim 1, wherein said MCH and said ICH within said computer system are components within a chipset.

3.   (Cancelled).

4.   (Previously Presented) The interface of claim 1, wherein said request packet includes a transaction descriptor.

5. (Previously Presented) The interface of claim 1, wherein a completion packet is transmitted on said interface in response to said request packet of said first transaction.

6. (Previously Presented) The interface of claim 1, wherein said request packet includes transaction descriptor and said completion packet includes a corresponding transaction descriptor.

7. (Original) The interface of claim 5, wherein a request packet for a second transaction can be transmitted across said interface prior to transmitting said completion packet in response to the request packet of said first transaction.

8. (Previously Presented) The interface of claim 1, wherein said data signal path is scalable.

9. (Original) The interface of claim 8, wherein packets are transmitted across said data signal path via a source synchronous clock mode.

10. (Original) The interface of claim 9, wherein said interface includes a set of bi-directional data signals, a first and second source synchronous strobe signal, a unidirectional arbitration signal, and a bi-directional stop signal.

11.   (Original) The interface of claim 10, wherein said interface further includes a system reset signal, a common clock signal, and a voltage reference signal.

12.   (Original) The interface of claim 11, wherein said transaction descriptors identify separate hubs within a hierarchy of multiple interfaces between at least three hubs.

13.   (Original) The interface of claim 5, wherein said request packet includes a field indicating if a completion packet is required in response to the respective request packet.

14.   (Previously Presented) The interface of claim 1, wherein arbitration between said hubs is symmetric and distributed.

15.   (Previously Presented) The interface of claim 1, wherein a hub is allotted ownership of said interface up to a predetermined amount of time.

16.   (Currently Amended) An single exclusive interface to transfer data directly between a memory control hub (MCH) and an input/ output control hub (ICH) within a computer system, comprising:

a first means for transmitting data between said MCH and said ICH in

packets via split transactions; and

a second means for transmitting command signals, wherein said interface

provides a point-to-point connection between said MCH and said ICH, exclusive

of an external bus connected directly to the interface, and peripheral components

only connected to MCH via the-a_single interface between the MCH and ICH.

17.   (Original) The interface of claim 16, wherein said ICH and said MCH

within said computer system are components within a chipset.

18.   (Original) The interface of claim 17, wherein said interface includes a

means for initiating a first transaction on said interface with a request packet.

19.   (Original) The interface of claim 18, wherein said request packet includes

a transaction descriptor.

20.   (Original) The interface of claim 19, wherein said interface includes means

for providing a completion packet in response to said request packet of said first

transaction.

21.   (Cancelled).

22. (Previously Presented) The interface of claim 16, wherein said interface includes a means for transmitting request packet for a second transaction across said interface prior to transmitting said completion packet in response to the request packet of said first transaction.

23. (Original) The interface of claim 22, wherein said first means for transmitting data in packets via split transactions includes further includes means for scaling a data signal path.

24. (Original) The interface of claim 23, wherein said interface includes means for transmitting packets across said interface via a source synchronous clock mode.

25. (Previously Presented) The interface of claim 16, wherein said transaction descriptors include a means for identifying separate hubs within a hierarchy of multiple interfaces between three or more hubs.

26. (Original) The interface of claim 20, wherein said request packet includes a means for indicating if a completion packet is required in response to the respective request packet.

27.   (Original) The interface of claim 26, wherein interface includes a means for

arbitrating between said hubs for ownership of said interface.

28.   (Previously Presented) The interface of claim 16, wherein said interface

further includes a means for is allotting ownership of said interface to one of said

hubs up to a predetermined amount of time.

29.   (Currently Amended) An single exclusive interface to transfer data

between a memory control hub and an input/output (I/O) hub of a chipset

within a computer system, comprising:

a bi-directional data signal path and a pair of source synchronous strobe

signals, said data signal path transmits data in packets via split transactions, said

packets including a request packet and completion packet, said request packet

including a transaction descriptor; and

a set of command signals including unidirectional arbitration signal, a bi-

directional stop signal, a system reset signal, a common clock signal, and a

voltage reference signal, wherein said interface provides a point-to-point

connection between said memory control hub and said I/O hub, exclusive of an

external bus connected directly to the point-to-point connection, and peripheral

components only connected to MCH via the a single interface between the MCH

and ICH.

30.   (Currently Amended) A computer system comprising

a processor;

a memory control hub (MCH) coupled to said processor;

an input/ output control hub (ICH) coupled to said MCH via ~~an~~ single

exclusive interface to transfer data directly between the MCH and the ICH;

said interface having a data signal path to transmit data in packets via

split transactions, and said interface including a set of command signals, wherein

said interface provides a point-to-point connection between said MCH and said

ICH, exclusive of an external bus connected directly to the point-to-point

connection, and peripheral components connected to MCH via ~~the~~-s single

interface between the MCH and ICH; and

a Peripheral Component Interconnect (PCI) agent~~at least one peripheral~~

~~component~~ coupled to said ICH.

31.   (Canceled)

32.   (Currently Amended) The computer system of claim 30~~1~~, wherein said

first and second hubs within said computer system are components within a

chipset.

33.   (Original) The computer system of claim 32, wherein a first transaction is initiated on said interface with a request packet, subsequent to arbitration for ownership of said interface.

34.   (Original) The computer system of claim 33, wherein said request packet includes a transaction descriptor.

35.   (Original) The computer system of claim 33, wherein a completion packet is transmitted on said interface in response to said request packet of said first transaction.

36.   (Cancelled).

37.   (Previously Presented) The computer system of claim 30, wherein a request packet for a second transaction can be transmitted across said interface prior to transmitting said completion packet in response to the request packet of said first transaction.

38.   (Previously Presented) The computer system of claim 30, wherein said data signal path is scalable.

39.   (Original) The computer system of claim 38, wherein packets are transmitted across said data signal path via a source synchronous clock mode.

40.   (Original) The computer system of claim 39, wherein said interface includes a set of bi- directional data signals, a first and second source synchronous strobe signal, a unidirectional arbitration signal, and a bi-directional stop signal.

41.   (Original) The computer system of claim 40, wherein said interface further includes a system reset signal, a common clock signal, and a voltage reference signal.

42.   (Original) The computer system of claim 41, wherein said transaction descriptors identify separate hubs within a hierarchy of multiple interfaces between at least three hubs.

43.   (Original) The computer system of claim 42, wherein said request packet includes a field indicating if a completion packet is required in response to the respective request packet.

44.   (Original) The computer system of claim 43, wherein arbitration between said hubs is symmetric and distributed.

45.   (Original) The computer system of claim 44, wherein a hub is allotted ownership of said interface up to a predetermined amount of time.

46.   (Original) The computer system of claim 3~~0~~1, wherein the computer system includes multiple processors.

47.   (Currently Amended) The computer system of claim 3~~0~~1, wherein the computer system further includes a third hub coupled to said ICH via an interface comprising:

        a bi-directional data signal path and a pair of source synchronous strobe signals, said data signal path transmits data in packets via split transactions, said packets including a request packet and completion packet, said request packet including a transaction descriptor; and

        a set of command signals including unidirectional arbitration signal, a bi-directional stop signal, a system reset signal, a common clock signal, and a voltage reference signal.

48.   (Currently Amended) The computer system of claim 3~~0~~1, wherein the processor and the MCH of said computer system, are integrated on a single semiconductor unit.

49.   (Currently Amended) The computer system of claim 3~~0~~1, wherein the

MCH and a graphics unit of said computer system, are integrated on a single

semiconductor unit.

50.   (Currently Amended) A memory control hub (MCH) comprising:

        a~~n~~ <u>single exclusive</u> interface to transfer data directly to an input/ output

control hub (ICH) within a computer system, the interface having a data signal

path to transmit data in packets via split transactions, and a set of command

signals, wherein the interface provides a point-to-point connection between said

the MCH and said ICH, exclusive of an external bus connected directly to the

interface, and peripheral components only connected to MCH via the single

interface between the MCH and ICH.

51.   (Original) The memory control hub of claim 50, wherein said MCH and

ICH are components within a chipset.

52.   (Original) The memory control hub of claim 50, wherein a first transaction

is initiated on said interface with a request packet, subsequent to arbitration for

ownership of said interface.

53.   (Original) The memory control hub of claim 52, wherein said request

packet includes a transaction descriptor.

54.   (Original) The memory control hub of claim 53, wherein a completion packet is transmitted on said interface in response to said request packet of said first transaction.

55.   (Original) The memory control hub of claim 52, wherein said request packet includes transaction descriptor and said completion packet includes a corresponding transaction descriptor.

56.   (Original) The memory control hub of claim 55, wherein a request packet for a second transaction can be transmitted across said interface prior to transmitting said completion packet in response to the request packet of said first transaction.

57.   (Original) The memory control hub of claim 56, wherein said data signal path is scalable.

58.   (Previously Presented) The memory control hub of claim 57, wherein packets are transmitted across said data signal path via a source synchronous clock mode.

59.   (Previously Presented) The memory control hub of claim 58, wherein said interface includes a set of bi- directional data signals, a first and second source synchronous strobe signal, a unidirectional arbitration signal, and a bi-directional stop signal.

60.   (Previously Presented) The memory control hub of claim 59, wherein said interface further includes a system reset signal, a common clock signal, and a voltage reference signal.

61.   (Previously Presented) The memory control hub of claim 60, wherein said transaction descriptors identify separate hubs within a hierarchy of multiple interfaces between at least three hubs.

62.   (Previously Presented) The memory control hub of claim 61, wherein said request packet includes a field indicating if a completion packet is required in response to the respective request packet.

63.   (Previously Presented) The memory control hub of claim 62, wherein arbitration between said hubs is symmetric and distributed.

64.   (Previously Presented) The memory control hub of claim 63, wherein a

hub is allotted ownership of said interface up to a predetermined amount of

time.

65.   (Previously Presented) The memory control hub of claim 50, wherein the

memory control hub and a processor are integrated on a single semiconductor

unit.

66.   (Previously Presented) The memory control hub of claim 50, wherein the

memory control hub and a graphics unit are integrated on a single

semiconductor unit.